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Patent and Trademark Offic
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/383,150	08/25/99	SHYU R	3576BP/S295

MM92/1022

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EXAMINER
ABRAHAM,F

ART UNIT	PAPER NUMBER
2826	# 11

DATE MAILED: 10/22/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/383,150	Applicant(s) SHYU, RONG-FUH	
	Examiner Fetsum Abraham	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

FETSUM ABRAHAM
PRIMARY EXAMINER

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Final Rejection

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-8, so far as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Raad in view of the prior art submitted by applicant in figure 1.**

Raad shows a fame composed of chips (103) having receiving section adjacent to both chips at the central portion and supplied with internal connection leads (111), and plurality of external terminals (12) attached to the chips for external connection, but omit to show how the external terminals are connected to the chips. However, figure 1 in the application shows that external connect terminals (13) are commonly connected with the chip through wires extended between the pads (110) on the chip and the external terminals. Therefore, it would have been obvious to one skilled in the art to use such a connection for all chips on a lead frame, since the method provides reliable wiring for IC chips..

Further, although the exact terms such as "windows" and "chip receiving windows" are not used by the prior art, it would have been obvious to one skilled in the art that the intention of the unclear terms are inherent to the structure because of structural similarity of the devices.

As for said master and slave ICs in claim 7 and the testing element in claim 8, the prior art does not discriminate such devices as the structure is applicable to any type of chips in the art.

Please note that the action is based on the fact that the interconnect structure in the prior art as being applicable for any type of device that cab be formed in a IC chips including memory, testing elements, and any other known ICs.

Claims 1-8, so far as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Mostafazadeh et al in view of the prior art submitted by applicant in figure 1.

Mostafazadeh et al show a fame (110) composed of chips (130) having receiving section adjacent to both chips at the central portion and supplied with internal connection leads, and plurality of external terminals or leads (120) attached to the chips for external connection. Although the prior art omits to show bonding pads on the chips, the lead frame in figures 1c-1-1d3 clearly suggests the existence of the bonds on the IC chips for connecting leads (140) with the chips similar to any lead frame structure (see column 1, 10-20). But, to the alternative, figure 1 in the application shows that external connect terminals (13) are commonly connected with the chip through wires extended between the pads (110) on the chip and the external terminals. Therefore, it would have been obvious to one skilled in the art to use such a connection for all chips on a lead frame, since the method provides reliable wiring for IC chips, and is the most basic interconnect methods in lead frames.

Further, although the exact terms such as "windows" and "chip receiving windows" are not used by the prior art, it would have been obvious to one skilled in the art that the intention of the unclear terms are inherent to the structure because of structural similarity of the devices.

As for said master and slave ICs in claim 7 and the testing element in claim 8, the prior art does not discriminate such devices as the structure is applicable to any type of chips in the art. Please note that the action is based on the fact that the interconnect structure in the prior art as being applicable for any type of device that cab be formed in a IC chips including memory, testing elements, and any other known Ics.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Please refer to PN: 5,796,746. The circuit in the patent has a testing circuit on the frame.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Examiner's comment on applicant's response

The applicant argues that the cited structures are distinct from each other and thus, their combination in rejected the claimed invention improper. This argument, however, is moot for the following explanations. The claim language duplicates the structure in figure 1 as is with modifications associated with the duplication. The modification is basically interconnecting the two similar devices through internal interconnect wires. That missing particular feature is the motivation for the action involving the second reference (Raad's). In light of this understanding, the action is believed to be appropriate.

Any inquiry concerning this communication should be directed to Fetsum Abraham at telephone number (703) 305-3793.

Fetsum Abraham

10/18/01

FETSUM ABRAHAM
PRIMARY EXAMINER